Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A data bridge system, comprising:

an interface for transferring data;

a plurality of application-specific integrated circuits (ASICs);

a data bridge operatively coupled to each: of the interface and the plurality of ASICs; and

the data bridge having a read only memory for storing at least initial values and mask values for each ASIC of the plurality of ASICs.

2. (Previously Presented) The data bridge system according to claim 1, wherein at least one of the plurality of ASICs is a graphic processor.

3. (Original) The data bridge system according to claim 1, wherein the interface is connected to a north bridge in a computer system.

4. (Original) The data bridge system according to claim 1, wherein the data bridge upon initialization forms at least one of: base address registers that are queried by the interface, command registers, and configuration registers.

5. (Original) The data bridge system according to claim 4, wherein the data bridge has six base address registers, each of the base address registers in the data bridge having a corresponding initial value and mask value that is stored in the read only memory.

6. (Original) The data bridge system according to claim 5, wherein the ASICs are graphic adapters, and wherein the initial values and the mask values stored in the read only

memory define the base address registers in the data bridge as a function of the configuration requirements of the graphic adapters.

7. (Original) The data bridge system according to claim 1, wherein the data bridge forms base address registers as a function of the initial values and mask values stored in the read only memory, and wherein a first base address register defines prefetchable memory space, a second base register address defines non-prefetchable memory space, and a third base address register defines I/O mapped space.

8. (Original) The data bridge system according to claim 1, wherein the data bridge has a plurality of base address registers that are programmable as a function of the initial values and mask values in the read only memory.

9. (Original) The data bridge system according to claim 1, wherein the read only memory is at least one of removably coupled to the data bridge and writable.

10. (Previously Presented) A method for configuring a plurality of ASICs in a multi-ASIC system comprising:

reading, initial values and mask values from a read only memory; and

forming, from the initial values and the mask values, configurable registers, that upon initialization of a system cause the system to allocate resources to each of the plurality of ASICs.

11. (Previously presented) The method according to claim 10,

wherein the computer system has an interface that, upon initialization of the computer system, writes all ones to base address registers of a data bridge and then reads back values to determine a size of a resource; and

wherein the computer system allocates memory space in the computer system as a function of the information in the base address registers.

12. (Original) The method according to claim 10, wherein the interface is connected to a north bridge in a computer system.

13. (Original) The method according to claim 10, wherein the data bridge has six base address registers, each of the base address registers in the data bridge having a corresponding initial value and mask value that is stored in the read only memory.

14. (Original) The method according to claim 13, wherein the ASICs are graphic adapters, and wherein the initial values and the mask values stored in the read only memory define the configuration registers in the data bridge as a function of the configuration requirements of the graphic processors.

15. (Original) The method according to claim 14, wherein the data bridge forms configuration registers as a function of the initial values and mask values stored in the read only memory, and wherein a first base address register defines prefetchable memory space, a second base register address defines non-prefetchable memory space, and a third base address register defines I/O mapped space.

16. (Original) The method according to claim 10, wherein the data bridge has a plurality of base address registers that are programmable as a function of the initial values and mask values in the read only memory.

17. (Original) The method according to claim 10, wherein the read only memory is at least one of removably coupled to the data bridge and is writable.

18. (Original) The method according to claim 10, wherein at least one of the plurality of ASICs is a graphic adapter.

19. (Original) A data bridge system, comprising:

an interface for transferring data;

a plurality of components;

a data bridge operatively coupled to each of the interface and the plurality of components; and

the data bridge having a storage device for storing at least initial values and mask values for each component of the plurality of components.

20. (Original) The data bridge system according to claim 19, wherein at least one of the plurality of components is a graphic adapter.

21. (Original) The data bridge system according to claim 19, wherein the interface is a north bridge in a computer system.

22. (Original) The data bridge system according to claim 19, wherein the data bridge upon initialization forms basic address registers that are queried by the interface.

23. (Original) The data bridge system according to claim 22, wherein the data bridge has six base address registers, each of the base address registers in the data bridge having a corresponding initial value and mask value that is stored in the storage device.

24. (Original) The data bridge system according to claim 23, wherein the components are graphic adapters, and wherein the initial values and the mask values stored in the storage

device define registers in the data bridge as a function of the configuration requirements of the graphic adapters.

25. (Original) The data bridge system according to claim 19, wherein the data bridge forms base address registers as a function of the initial values and mask values stored in the storage device, and wherein a first base address register defines prefetchable memory space, a second base register address defines non-prefetchable memory space, and a third base address register defines I/O mapped space.

26. (Original) The data bridge system according to claim 19, wherein the data bridge has a plurality of base address registers that are programmable as a function of the initial values and mask values in the storage device.

27. (Original) The data bridge system according to claim 19, wherein the read only memory is removably coupled to the data bridge.

28. (Previously presented) A circuit comprising:

memory containing initial values and mask values for use in forming a register; and

at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory.

29. (Canceled)

30. (Currently amended) The circuit of claim [[29]]36 wherein the mask flop is operatively responsive to the mask value and a mask write enable signal.

31. (Original) The circuit of claim 30 operatively coupled to a computer system such that upon initialization of the computer system, the computer system allocates system resources to each of a plurality of ASICs based on the initial values.

32. (Cancelled)

33. (Previously Presented) The method according to claim 10 wherein at least a plurality of the ASICs are graphic processors, and wherein the initial values and mask values stored in the read only memory define the configuration registers in the data bridge as a function of the configuration requirements of the plurality of graphic processors.

34. (Previously presented) The data bridge system of claim 1 comprising at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory.

35. (Previously presented) The method according to claim 10 wherein forming the configurable registers comprises forming at least one register flop of the configurable register to be read and/or writable based on at least one mask value.

36. (New) A circuit comprising:

memory containing initial values and mask values for use in forming a register;

at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask flop that generates a mask bit for the

configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based on at least one mask value stored in the memory;

wherein the configuration logic includes:

a multiplexing circuit operatively responsive to the initial value and write data,

an AND gate operatively responsive to a register write enable signal and to the mask bit,

an OR gate operatively coupled to receive an output from the AND gate and operatively responsive to an initial write enable signal and a reset signal, and

a NAND gate operatively coupled to the multiplexing circuit and operatively responsive to the reset signal and having an output operatively coupled to the register flop.